VERSION OF SPECIFICATION AND CLAIMS AMENDMENTS
WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 1, before the title, please delete the heading "Specification".

Page 1, paragraph [0001]:
[0001] The present invention relates to a data transmission system [according to the definition of the species in Claim 1] for serial asynchronous data transmission between two devices.

Page 1, paragraph [0003]:
[0003] Therefore, [the] an object of the present invention is to provide a data transmission system which [ensures a] achieves serial asynchronous data transmission with a small technical effort.

Page 1, paragraph [0005]:
[0005] The power supply to the [preferably galvanically separated] circuit part, which may be galvanically separated, of the first device [(preferably master device)], which may be a master device, via the bus side is ensured according to the present invention by feeding a current, in particular a constant current, into the [only] single, bidirectional data transmission line of the system.

Page 2, paragraph [0009]:

[0009] Further details and advantages of the present invention [ensue from the following exemplary embodiment which will be explained in the following on the basis of Figures.] will be elaborated upon below based on exemplary embodiments with reference to the drawings, in which:

Page 2, paragraph [0010]:

[0010] Figure 1 [is] shows a schematic representation of a data transmission system according to the present invention;

Figure 2: [depicts a possible] shows a schematic representation of an embodiment of a data transmission system according to Fig. 1; and

Figure 3 shows a schematic representation of a data transmission system [in a further possible embodiment] according to another embodiment of the present invention.

Page 2, paragraph [0011]:

[0011] According to Fig. 1, [the] a data transmission system according to the present invention includes two circuit parts which can be interconnected via a two-pole line 8.

Page 4, paragraph [0017]:

[0017] Transmitter- and receiver circuit parts 4a, 4b of circuit part 4 assigned to expansion unit 3 each have a semiconductor switch T1, T3, [preferably] which may be an n-p-n switching transistor. In this connection, transmitter terminal Tx_Ew is connected via an ohmic resistance to the base of a transistor T3. The emitter of transistor T3 is connected to reference potential ground (GND) and connectable via reference potential line 8a to circuit part 2 assigned to basic unit 1. The collector of transmitter resistor T3 is connected, via a Zener diode D1 and a resistor R1 connected in series thereto, to the base of transistor T1 of receiver circuit part 4b and is moreover connected to power supply 6 for the purpose of current impression. Via the collector of transistor T3, moreover, circuit part 4, which is assigned to expansion unit 3, is connectable

via data transmission line 8b to circuit part 2, which is assigned to basic unit 2. Receiver terminal Rx_Ew [is constituted by] may include the collector of transistor T1, the collector being pulled to 5V via a pull-up resistor. The emitter of transistor T1 is connected to ground potential.

Page 4, paragraph [0018]:

[0018] Power supply 6 [is preferably constituted] may include by a p-n-p transistor T2 which is connected on the emitter side to a supply potential (here 24 V) via an ohmic resistor R2, transistor T2, on the base side, being also connected to the supply potential via a Zener diode D2 as well as to the reference potential via a further ohmic resistor and, via its collector terminal, to data transmission line 8b.

Page 4, paragraph [0020]:

[0020] The base of transistor T2 is supplied via a voltage divider [constituted by] including a Zener diode D2 and a resistor, Zener diode D2 being connected to +24V on the cathode side and to ground potential via the resistor on the anode side.

Page 5, paragraph [0021]:

[0021] Transmitter- and receiver circuit parts 2a, 2b of circuit part 2 assigned to basic unit 1 [are preferably] may also built with semiconductor switches Opto1, Opto2. In the [exemplary] embodiment shown, these semiconductor switches are designed as circuit elements which ensure a galvanic separation, preferably as optocouplers [Opto1; Opto2] Opto1, Opto2. Receiver circuit part 2b [is composed of] includes an optocoupler (Opto2) which is connected to ground potential via its emitter on the transistor side (with n-p-n transistor stage). The collector is connected to Vcc potential (here approximately 5V) via a pull-up resistor and, at the same time, [constitutes] is included in the receiver terminal RX_CPU on the side of the basic unit. terminal Rx_Ew may include the collector of transistor T1, the collector being pulled to 5V via a pull-up resistor. The emitter of transistor T1 is connected to ground potential.

Page 5, paragraph [0025]:

[0025] In the rest state of the data transmission system, output transistors T3 or T_Opto1 (transistor of optocoupler Opto1) of the two transmitter circuit parts 2a, 4a, respectively, are blocked (collector-emitter path non-conducting). Impressed current Iq is divided between the two receiver circuit parts 2b, 4b. In this context, the data transmission system [is preferably] may be dimensioned in such a manner that the largest portion of the current flows through data transmission line 8b and through the receiver circuit part 2b (D3, D_Opto2 (diode of second optocoupler Opto2)) assigned to basic unit 1. In this manner, the susceptibility to failure of the circuit is minimized.

Page 6, paragraph [0026]:

[0026] In [the exemplarily depicted] power supply 6, featuring Zener diode D2 and transistor T2, the current is:

$$Iq = V_{R2}/R2 = (V_{D2} - V_{EB\_T2})/R2$$

Page 8, paragraph [0042]:

[0042] In [a preferred] an embodiment of the present invention, transmitter- and receiver circuit parts (2a, 2b) are designed as elements which ensure a galvanic separation, [preferably as] and may be optocouplers (Opto1, Opto2). Transmitter- and receiver circuit parts (4a, 4b) [are preferably] may be designed in the form of transistor stages.

Page 8, paragraph [0043]:

[0043] The present invention is not limited to the [specific] embodiments described above but includes all [equally acting embodiments along the lines of the present invention] variations within the scope of the appended claims. Thus, the present invention can also be implemented using other semiconductor switch elements, operational amplifiers, or the like.

Page 9 first line : --WHAT IS CLAIMED IS-- [What is claimed is].

2/pats

Specification

DATA TRANSMISSION SYSTEM

[0001] The present invention relates to a data transmission system according to the definition of the species in Claim 1.

[0002] A serial data transmission system of this kind is known, for example, through the ASI bus system (actuator-sensor interface). The stations of this bus system are actuators and sensors of the most different kinds. All devices that are connected to such a system must have an appropriate intelligence in the form of a microcontroller or an ASIC as well as a compatible device interface. The communication between the stations of the bus and the power supply to the stations are carried out via a double-core, unshielded cable. To this end, the data is transmitted in modulated form via the supply voltage. For a reliable data transmission, specially developed ASIC modules are used in the stations of the ASI bus system. In the past, such a design approach has proven to be efficient but is technically too complex and too expensive for smaller systems.

[0003] Therefore, the object of the present invention is to provide a data transmission system which ensures a serial asynchronous data transmission with a small technical effort.

[0004] On the basis of a data transmission system of the type mentioned at the outset, this objective is achieved according to the present invention by the characterizing features of the independent claim while advantageous refinements of the present invention can be gathered from the dependent claims.

[0005] The power supply to the preferably galvanically separated circuit part of the first device (preferably master device) via the bus side is ensured according to the present invention by feeding a current, in particular a constant current, into the only, bidirectional data transmission line of the system.

[0006] For example, in the case of the communication between a master device and a slave device, the power supply to both devices is generally ensured via the power supply unit of the master device.

[0007] According to the present invention, the power supply unit of the master device is advantageously relieved by feeding in a current, preferably in the form of a constant current, and by the so implemented supply to the circuit part on the bus side. Due to this, a power supply unit having galvanically separated supply terminals for bus-side and device-side circuit parts of the master device can be dispensed with. In the preferred embodiment of the present invention, the transmitter- and receiver circuit parts of the slave device are designed to have conventional transistors (here n-p-n transistors) and the transmitter- and receiver circuit parts of the master device are designed to have optocouplers which are suitable for the galvanic separation.

[0008] The two circuit parts can be designed as separate coupling modules for connection to intelligent switching or control devices, or else as separate coupling modules for coupling control devices with expansion modules which are connectable thereto, or the like.

[0009] Further details and advantages of the present invention ensue from the following exemplary embodiment which will be explained in the following on the basis of Figures.

[0010] Figure 1 is a schematic representation of a data transmission system according to the present invention;

Figure 2: depicts a possible embodiment of a data transmission system according to Fig. 1; and

Figure 3 shows a data transmission system in a further possible embodiment.

[0011] According to Fig. 1, the data transmission system according to the present invention

includes two circuit parts which can be interconnected via a two-pole line 8.

[0012] A first circuit part 2 is used for the coupling to a basic unit 1 (master), in particular, a programmable small control system such as logic relays or the like. A small control system of that kind includes, in particular, a microcontroller, a display unit, an operating control unit, signal inputs and signal outputs, the processing unit, the display screen, the operating control unit, the signal inputs and the signal outputs being accommodated in a common housing.

[0013] A second circuit part 4 is used for the coupling to an expansion unit 3 (slave) which can be connected to basic unit 1. Circuit parts 2 and 4 can be integrated in the respective devices 1 and 3 or designed as separate circuit modules.

[0014] Circuit part 2, which is assigned to basic unit 1, is composed of a transmitter circuit part 2a and a receiver circuit part 2b, the two elements being preferably designed in such a manner that a galvanic separation between inputs and outputs of the circuit parts is guaranteed. Circuit part 4, which is assigned to expansion unit 3, is also composed of a transmitter circuit part 4a and a receiver circuit part 4b. In the exemplary embodiment shown, moreover, a power supply 6 is integrated in the circuit part 4 assigned to expansion unit 3. Alternatively, power supply 6 can also be external or configured in circuit part 2 of basic unit 1.

[0015] Circuit parts 2, 4 can be interconnected via two-pole connecting line 8, one of the lines 8a carrying a reference potential, here ground (GND), and the other line 8b being used as a data transmission line. The data is transmitted by the two devices 1, 3 via the only data line 8b, which is therefore intended for the bidirectional data traffic. An appropriate communication protocol ensures that a collision of data is prevented. According to the present invention, a current Iq (preferably a constant current) is impressed upon data line 8b via power supply 6. This current Iq is used, in addition to the data transmission, for the power supply to the galvanically separated subsections of connected circuit parts 2a, 2b. Moreover, the current (Iq) makes it possible that, depending on input signals of the

transmitter circuit parts of one device 1,3, received signal conditions of the other device 3,1 can be changed.

[0016] Design of the circuit configuration according to Fig. 2:

[0017] Transmitter- and receiver circuit parts 4a, 4b of circuit part 4 assigned to expansion unit 3 each have a semiconductor switch T1, T3, preferably an n-p-n switching transistor. In this connection, transmitter terminal Tx_Ew is connected via an ohmic resistance to the base of a transistor T3. The emitter of transistor T3 is connected to reference potential ground (GND) and connectable via reference potential line 8a to circuit part 2 assigned to basic unit 1. The collector of transmitter resistor T3 is connected, via a Zener diode D1 and a resistor R1 connected in series thereto, to the base of transistor T1 of receiver circuit part 4b and is moreover connected to power supply 6 for the purpose of current impression. Via the collector of transistor T3, moreover, circuit part 4, which is assigned to expansion unit 3, is connectable via data transmission line 8b to circuit part 2, which is assigned to basic unit 2. Receiver terminal Rx_Ew is constituted by the collector of transistor T1, the collector being pulled to 5V via a pull-up resistor. The emitter of transistor T1 is connected to ground potential.

[0018] Power supply 6 is preferably constituted by a p-n-p transistor T2 which is connected on the emitter side to a supply potential (here 24 V) via an ohmic resistor R2, transistor T2, on the base side, being also connected to the supply potential via a Zener diode D2 as well as to the reference potential via a further ohmic resistor and, via its collector terminal, to data transmission line 8b.

[0019] In a simplified embodiment, it is also possible for the power supply to be constituted by an ohmic resistor which is connected to a supply potential via one end and to data transmission line 8b via the other end. The power supply is advantageously integrated in slave device 3.

[0020] The base of transistor T2 is supplied via a voltage divider constituted by a Zener diode D2 and a resistor, Zener diode D2 being connected to +24V on the cathode side and to ground potential via the resistor on the anode side.

[0021] Transmitter- and receiver circuit parts 2a, 2b of circuit part 2 assigned to basic unit 1 are preferably also built with semiconductor switches Opto1, Opto2. In the exemplary embodiment shown, these semiconductor switches are designed as circuit elements which ensure a galvanic separation, preferably as optocouplers Opto1; Opto2. Receiver circuit part 2b is composed of an optocoupler (Opto2) which is connected to ground potential via its emitter on the transistor side (with n-p-n transistor stage). The collector is connected to Vcc potential (here approximately 5V) via a pull-up resistor and, at the same time, constitutes the receiver terminal RX_CPU on the side of the basic unit.

[0022] On the diode side, optocoupler Opto2 is connected via its cathode to the emitter of optocoupler (with n-p-n transistor stage) Opto1 of transmitter circuit part 2a and is connectable to circuit part 4 of expansion unit 3 via reference potential line 8a. Via its anode, optocoupler Opto2 of receiver circuit part 2b is connected to the collector of optocoupler Opto1 of transmitter circuit part 2a via a Zener diode D3 arranged in forward conducting direction and is connectable to circuit part 4 of expansion unit 3 via data transmission line 8b.

[0023] On the diode side, the anode of optocoupler Opto1 is connected to transmitter input Tx_CPU via a resistor. On the cathode side, optocoupler Opto1 is connected to ground potential.

[0024] Mode of operation of the circuit configuration according to Fig. 2:

[0025] In the rest state of the data transmission system, output transistors T3 or T_Opto1 (transistor of optocoupler Opto1) of the two transmitter circuit parts 2a, 4a, respectively, are blocked (collector-emitter path non-conducting). Impressed current Iq is divided between the two receiver circuit parts 2b, 4b. In this context, the data transmission system is preferably dimensioned in such a manner that the largest portion of the current flows through data

transmission line 8b and through the receiver circuit part 2b (D3, D_Opto2 (diode of second optocoupler Opto2)) assigned to basic unit 1. In this manner, the susceptibility to failure of the circuit is minimized.

[0026] In the exemplarily depicted power supply 6 featuring Zener diode D2 and transistor T2, the current is:

$$Iq = V_{R2}/R2 = (V_{D2} - V_{EB\_T2})/R2$$

[0027] Zener diode D3 determines the voltage level of data transmission line 8b in the rest state (signal inactive, logical "0"):

$$V_{L\_REST} = V_{D3} + V_{D\_Opto2}$$

[0028] The current through receiver circuit part 4b assigned to expansion unit 3 is determined by Zener diode D1 and resistor R1:

$$I1 = V_{R1}/R1 = (V_{L\_REST} - V_{D1} - V_{BE\_T1})/R1$$

[0029] The data flow then takes place as follows:

[0030] Transmitter circuit part 2a/basic unit 1 transmitting - receiver circuit part 4b/expansion unit 3 receiving:

[0031] As long as the transmitted bit is logically "0" (Tx_CPU = 0), data transmission line 8b remains inactive, that is in the rest state as described above.

[0032] If the intention is to transmit a "1"-signal, then output transistor T_Opto1 of transmitter circuit part 2a opens and the entire current Iq flows back from power supply 6 to the ground potential via data transmission line 8b, transistor T_Opto1 and the ground line

(reference potential line 8a). The voltage level of data transmission line 8b is nearly 0V (collector-emitter voltage of optocopler Opto1 in the enabled condition $V_{CE\_SAT\_T\_Opto1} \approx$ 0.2V).

[0033] Since current can no longer flow through Zener diode D1 via R1 and the base T1 (D1 is blocked), receiver transistor T1 flips states (blocks, Rx_Ew = 1) so that receiver terminal Rx_Ew of expansion unit 3 switches from logical 0 to logical 1.

[0034] At the same time, current no longer flows through Zener diode D3 and diode D_Opto2 of optocoupler Opto2, and the transistor of receiver optocoupler T_Opto2 flips states as well (blocks, Rx_CPU = 1). In this manner, basic unit 1 gets feedback which can be used for checking purposes.

[0035] Transmitter circuit part 4a/expansion unit 3 transmitting - receiver circuit part 2b/basic unit 1 receiving:

[0036] As long as the transmitted bit is logically "0" (Tx_CPU = 0), data transmission line 8b remains inactive, that is in the rest state as described above.

[0037] If the intension is to transmit a "1"-signal, then transmitter transistor T3 in the expansion module opens and the entire current Iq flows from power supply 6 to the ground potential via transistor T3. The voltage level of data transmission line 8b is nearly 0V (collector-emitter voltage of enabled transistor T3 $V_{CE\_SAT\_T\_T3} \approx$ 0.2V).

[0038] Since current can no longer flow through Zener diode D3 and diode D_Opto2 of optocoupler Opto2 (D3 is blocked), transistor T_Opto2 of optocoupler Opto2 flips states and blocks so that the signal changes from logical 0 to logical 1 at receiver terminal Rx_CPU of the basic unit.

[0039] At the same time, current no longer flows through Zener diode D1 via R1 and the

base of T1 either, and receiver transistor T1 blocks as well so that the signal changes from logical 0 to logical 1 at receiver terminal Rx_Ew of expansion unit 3. In this manner, expansion unit 3 gets feedback which can be used for checking purposes.

[0040] According to the present invention, the data transmission system is designed in such a manner that the normal working currents are also used as "power supply" for the galvanically separated circuit parts of the basic unit which are located on the side of the connecting line (bus side). This configuration is particularly suitable for asynchronous transmission modes.

[0041] In practice, additional components in the form of filters and amplifier stages are needed. A circuit which is optimized in this manner is illustrated in Fig. 3.

[0042] In a preferred embodiment of the present invention, transmitter- and receiver circuit parts (2a, 2b) are designed as elements which ensure a galvanic separation, preferably as optocouplers (Opto1, Opto2). Transmitter- and receiver circuit parts (4a, 4b) are preferably designed in the form of transistor stages.

[0043] The present invention is not limited to the specific embodiments described above but includes all equally acting embodiments along the lines of the present invention. Thus, the present invention can also be implemented using other semiconductor switch elements, operational amplifiers, or the like.